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Summary of Research For:

Phase-Locked Output Control of

High Voltage Power Supplies

Work Performed Under:

NASA Planetary Instrumentation Definition and

Development Program

Grant: NAGW-4595

Period of Performance: June, 1995 through May, 1997

Principal Investigator:

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1. Introduction

The research and prototype development effort performed under NASA grant NAGW-4595, "Phase-Locked Output Control of High Voltage Power Supplies", was initiated due to the need for low-power, high voltage power supplies in space science instruments, such as charged particle analyzers. It was recognized that a voltage sensor which did not dissipate power from a high voltage converter would be helpful in reducing the input power to the system. Conventional systems used a resistive divider for sensing the output voltage, which was often a significant part of the output load. Features such as isolation of high voltage and control system grounds were also frequently required. The author was made aware of these needs during work on HV systems us on sounding rockets and on the WIND, POLAR, and ACE satellites.

2. History of the Phase-Locked HV Control Concept

The author had been involved in the development of high voltage supplies for several years before beginning this project. An especially useful development in "stepping" output high voltage supplies was the optoelectronic output stage originated by the Germans [1], which was adapted by the author for sounding rocket use, and by NASA for satellite use. This output stage was also adapted for use in the high voltage stepper prototype, described below.

The author implemented an electro-optic high voltage sensor to monitor a high voltage supply using a Pockels cell in 1992. NASA/JPL published articles describing polymer-based electro-optic cells in November, 1992 [2, 3]. Further investigation of electro-optic materials as nonlinear dielectrics led to the consideration of ferroelectric substances [4] as voltage sensors. Commercial literature [5] showed that off-the-shelf barium titanate capacitors had a large voltage coefficient, and might be used as part of a voltage sensing network, or tank circuit. A phase-locked loop control system could be used take advantage of this sensor. This led to the proposal for this grant, awarded in 1995.

3. Overview of Research and Development

The research and development effort included characterization of nonlinear capacitors for use as voltage sensors, prototype design, prototype construction, and testing. A brief overview of the work follows.

Design of the control system, other than the high voltage sensor itself, was simplified by the use off-the-shelf integrated circuits. Due to the large demand for phase-locked loop (PLL) control circuits in wireless devices, single-chip PLL controllers were available for use, one of which is described in reference [6]. The control system was reduced to just a few integrated circuits and support components, and high level control of the PLL system was achieved by sending data to the PLL control IC over a computer printer port interface. Prototype circuits were developed to demonstrate the closed-loop operation of a phase-locked high voltage control system.

A block diagram of the control system is attached to this summary and shows the PLL IC functions, HV converter, optoelectronic output stage, and high voltage sense network.

The heart of the system was the high voltage controlled oscillatc or "HVCO". This circuit provided an output frequency related to the high voltage bias applied to the sensing network, which was part of the oscillator tank circuit. Several test oscillators were constructe in order to check candidate capacitors over a range of input voltages and temperatures. As expected, the oscillators showed considerable temperature sensitivity. For one of the prototypes, the voltage sensitivity was roughly 66 Hz/volt in the 1000 to 2000 volt range. At a bias level of 1500 volts, the temperature coefficient was about -53 Hz/degree Celsius, causing frequency to decrease from 1630 kHz as temperature increased above 25 degrees Celsius. Less expected was a sign change in the voltage sensitivity at a bias level of several hundred volts. The low voltage region of operation had to be avoided in order to maintain system stability. Applying a clean, differential bias voltage to the HVCO was suggested as a means of extending the effective operating range of the HVCO to lower voltages.

Due to the sensitivity variations observed in the HVCO circuits, simple temperature compensation was felt to be of limited utility; calibration of the sensors over expected bias and temperature ranges was recommended as the way to prepare for their use. Still, the methc used to construct LC oscillators for communications use [7] were felt to be of value, since sources of frequency drift other than those attributed to the HV-sensing capacitors could be minimized. The eventual use of ceramic transmission line resonators, and of a temperature sensor and a microcontroller to handle temperature corrections, were pointed out as items for possible future developmen

Other dielectrics for nonlinear capacitors, and different additiv to barium titanate, were found in references [8], [9], and [10] durin research into this issue. Also, the question of using non-ferroelectr materials was raised; it was found that most "ordinary" dielectrics are nonlinear only in the case of extremely large electric fields [11 so large as to be impractical. Good general references on dielectrics were found to be [12] and [13].

4. Conclusions

The use of phase-locked control techniques was demonstrated in a prototype stepping (programmable output) high voltage supply. The high voltage sensors constructed had useful voltage coefficients, but also showed temperature sensitivity. With proper calibration over temperature and applied bias, such sensors could find use in situations where power from a high voltage converter was available only at a premium, and where loads consisted of a small capacitances, such as the deflection plates of charged particle analyzers.

5. Publications and Other Media

A high-level description of the phase-locked high voltage control system is scheduled to be published in the July, 1997 issue of NASA Tech Briefs at the time of this writing. A technical support/ final report package, containing more details concerning the design of the prototype stepper, is being prepared at this time, and will be made available to those interested upon request.

6. References

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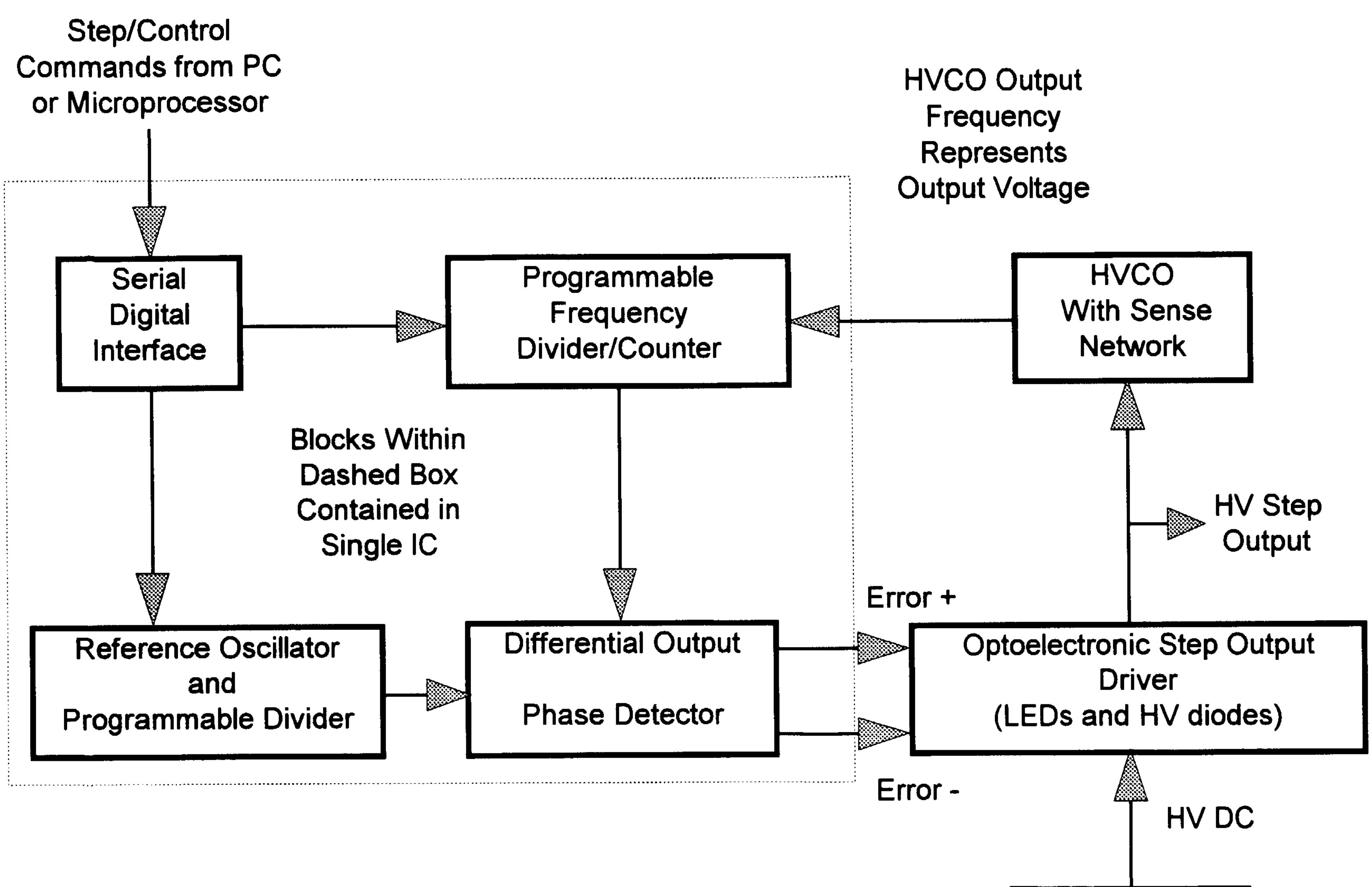

Attachment: Phase-Locked High Voltage Control System

Final Report For:

Phase-Locked Output Control of High Voltage Power Supplies

Work Performed Under:

NASA Planetary Instrumentation Definition and Development Program

Grant: NAGW-4595

Period of Performance: June, 1995 through May, 1997

Principal Investigator:

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Contents

1. Introduction

This report summarizes the research performed under NASA grant NAGW-4595, "Phase-Locked Output Control of High Voltage Power Supplies", within NASA's Planetary Instrument Definition and Development Program. The period of performance covered is that of the entire grant, beginning in June, 1995, and continuing through May, 1997. The project has historical ties to related work by the author in the area of high voltage supplies for space science applications, as described below.

2. A History of Phase-Locked HV Power Supply Control

For approximately ten years, the author has been active in the development of high voltage power supplies for use in space science instruments on board sounding rockets and satellites, including WIND, POLAR, and the Advanced Composition Explorer (ACE) satellites with the University of New Hampshire Space Science Center. The eighties saw some new developments in high voltage control systems, such as optoelectronic output control [1], where the reverse-bias current of high voltage diodes was controlled by by illumination with infrared light. This technique was developed by the Germans for use on the Giotto mission, adapted by the author for use on sounding rockets, and used by NASA for the WIND and POLAR satellites. Optoelectronic control has provided for the implementatio of simple, well-behaved, inexpensive, and robust high voltage supplie for many projects.

Many times during the development and testing of these supplies, someone would ask the question: "Why is more input power required to operate the supply at the higher output voltage steps? The load is a capacitance." The answer was that the "load" presented by the resistive divider inside the high voltage supply dissipated more power at the high voltage steps. This divider was needed in order to produce a low-level analog of the high voltage output for control purposes. Even though high value (on the order of 1.0E9 Ohm) resistors were often used in order to reduce this power consumption, the power dissipated was significant and observable. One could not continue to increase the divider resistance in order to reduce power consumption; problems with DC errors due to op-amp bias currents and stray capacitances affecting the divider network frequency response prevented this.

These questions and problems, along with some unrelated work on a fiber-optic system being performed by the author, led to the consideration of the use of electro-optic crystals as voltage sensors in 1992, which was even the subject of an SBIR proposal. Later that year, NASA/JPL published reports on using an electro-optic polymer as a high voltage sensor [2], [3].

After building a prototype sensor based on a Pockels cell and testing it, it was realized that electro-optic sensors were expensive and required careful adjustment, along with an optical source, polarizing and analyzing optics, and support electronics to convert the polarization state of the optical sensor output into a useful error signal for the control system.

The work done on electro-optic sensors led to further thought on the subject of a voltage sensor built of an insulating material. Since the electro-optic effect was a change in the (optical frequency) dielectric constant of a material due to an applied electric field, it was recalled that many of the electro-optic materials were also ferroelectric, and showed a large dependence of dielectric constant upon the applied electric field at DC and radio frequencies [4]. This implied that a voltage sensor might be built using a capacitor with a ferroelectric material between the plates, and suitable electronics to detect the capacitance changes due to changes in applied voltage. A straightforward means of detecting the capacitance changes would be to include the ferroelectric capacitors in an oscillator tank circuit whose resonant frequency would depend on the value of the capacitance. Such an arrangement would lend itself to the use of phase-locked loop techniques in the monitoring and control of high voltage power supplies.

The sensitivity of barium titanate capacitors to DC bias became very apparent during discussions with the University of New Hampshire Space Science Center concerning problems they had in the design of a 30 kilovolt Cockroft-Walton multiplier stack. The multiplier had "refused" to reach the desired 30 kilovolt output level until the capacitors were changed to "NPO" dielectric units which were insensitive to DC bias, even near rated voltage. This led to the review of some commercial data [5] which showed a decrease in capacitance of about 25% as rated voltage was approached in certain barium titanate capacitors. Thus, it was possible to obtain candidate "voltage sensors" readily from commercial sources.

The only apparent drawback to using ferroelectric materials in voltage sensors was the fact that the relative dielectric constant of such materials depended not only upon the applied electric field, but also upon temperature. It was seen that the temperature dependence would need to be compensated for if a voltage sensor was to be useful in a space application. In reviewing the commercial literature, it was found that capacitors designated as having an "X7R" dielectric showed combination of manageable temperature coefficient and usable voltage coefficient. It was also known that LC oscillators of high stability had been produced for communications purposes for many years, so that the temperature coefficient problem could possibly be reduced by using temperature compensation techniques. The use of calibration tables and microcontrollers was also a possibility.

Consideration of how to use the sensor led to the concept of a phase-locked control system, where the sensor would take the place of the voltage-controlled oscillator (VCO) in a typical PLL. In such a system, the output frequency of the VCO would represent the high voltage at the output. It would be compared to another frequency, or reference, in a phase/frequency detector circuit. The output of the detector would be an error signal which would be filtered and used to control the high voltage output.

At that point, in the summer of 1994, it was felt that the concept of a capacitive voltage sensor was technically sound enough to be worth proposing a development effort. The Planetary Instrument Definition and Development Program, which allowed for the design and breadboarding of new instrument concepts, was a proper vehicle for the development. A proposal was submitted in the fall of 1994, which led to this grant and development effort.

The proposed efforts included:

(1) Characterization of High Voltage Capacitors As Voltage Sensors

This work included the selection and temperature testing of capacitors for use in the high voltage controlled oscillator (HVCO) circuits. Some consideration was given to the material properties which caused the capacitors to have values dependent upon bias voltage. Plots showing the results of some temperature tests are described later in this report, and appear in the Attachments section.

(2) High Voltage Control System Design

Using the information from task 1, high voltage control systems using phase-locked control techniques were designed, with emphasis on high voltage "stepping". A block diagram of such a stepping system is described in this report, and appears in the Attachments section.

(3) Prototype Construction and Testing

In order to verify the "paper" designs, prototype high voltage control systems were constructed and tested. This was the heart of the project. Schematics for the prototype stepper system are provided as part of this report.

(4) Report Preparation

In the interest of serving the space science community and fulfilling the purpose of the Planetary Instrument Definition and Development Program, design information for the phase-locked high voltage control systems is presented in this report. Additional systems-level information is to be published in a NASA Tech Briefs article (scheduled for the July, 1997 issue at the time of this writing).

Rather than a strictly chronological account of the tasks involved in developing the PLL high voltage prototype, a description of the PLL system will be given first, followed by design details and test results.

3. The Phase-Locked High Voltage Control System

Figure 1 in the Attachments shows a block diagram of one version of the high voltage control system, configured as a "stepper". The functional blocks in the diagram can be related directly to a conventional stepper control system as follows:

Function	PLL Stepper	Conventional Stepper
Voltage reference	Quartz crystal	Voltage reference IC
Step level control	Reference frequency divider	DAC or resistors and analog switches
Error junction	Phase detector	Op-amp differential input
Feedback signal	HVCO and frequency divider	Resistive divider
HV source	Inverter/Stack	Inverter/Stack
Output control	LEDs/HV diodes	LEDs/HV diodes

The conceptual difference between the two approaches is the use c frequency to represent the HV output within the phase-locked control system, as opposed to the use of a low-voltage analog of the high-voltage output in a conventional system. Note that the HV source and stepper output control stages are shown as the same for both example systems. The use of some type of inverter (oscillator and transforme to produce a moderately high voltage AC waveform is common to most systems. The "stack", or Cockroft-Walton multiplier, converts the high voltage AC to a much higher DC level. The method of output cont shown is an optoelectronic output stage, which, as mentioned earlier, has proven to be useful for driving small capacitive loads in space science instruments. It is not the only method of controlling the high voltage output, however.

For instance, a predecessor to the "stepper" prototype was a PLL-based high voltage supply which did not have the LED/HV diode output stage. Instead, the PLL phase detector output (error signal) was filtered and used to control the HV converter oscillator bias directly. Since any changes in output voltage required that the Cockroft-Walton stack had to be charged or discharged, the output changed very slowly. With no resistive load, except for the high voltage test probe, it was observed that down-steps were much slower than up-steps; this was due to the lack of any means of actively reducing the output level- any reductions were due to leakages in the stack diodes, capacitors, and the probe resistance. The optoelectronic stage overcame this problem by providing both series ("pull up") and shunt ("pull down") control elements, so that up- and down-steps had similar speeds.

4. Small-Signal Model

For a quick stability check, a small-signal model of the PLL control system elements can be constructed from the following:

Phase detector:	5/(2*pi)	[V/rad]
LED/HV diodes:	2/100000	[A/V]
HVCO input Z:	1/(s*(C12+C13))	[Ohms]
Damping Z:	R23+1/(s*C38)	[Ohms]
HVCO gain:	(100kHz*2*pi/1200V)/s	[((rad/sec)/V)*sec]
Frequency divider:	1/2000	[unitless]

In the above expressions, "s" is the complex frequency variable. The phase detector gain is taken from the PLL device data [6].

The LED/HV diode stage gain is a linearized estimate, found as follows. The phase detector outputs actually consist of 0 to 5V (CMOS logic) pulses whose width represents the phase error. These are converted to pulses with a maximum amplitude of 15V by the LED driver. The peak LED current is limited by a resistor and the forward drops of the LEDs to be less than 100 mA. Experience has shown that the current transfer ratio of the LED/HV diode optoelectronic output stage to be about 1/1000, that is, 1 microampere of output current for each milliampere of LED current. The HV diodes are considered to behave like current sources. So, when the phase detector is producing a 5V pulse, the photocurrent in the HV diodes is 100 microamperes, for an estimated gain of (1.0E-4 A / 5 V), or 2.0E-5 A/V.

This photocurrent is drawn from the high voltage converter and drives HVCO input and "damping" impedances, which must be considered in parallel in the model:

$$Zeq = (1/s)*(s*Cd*Rd + 1)/(Cv + s*Cv*Cd*Rd)$$

where Rd = R23, Cd = C38, and Cv = C12 + C13 (schematic references).

The main difference in the analysis of the HV PLL system and a conventional PLL is the consideration of this impedance. However, a conventional PLL contains a loop filter transfer function in this part of the system. The "damping" impedance and HVCO input impedance take the place of the loop filter, and modifications to this part of the circuit can be made to adjust system frequency response and time domain behavior.

The HVCO gain includes a 1/s factor (an integrator), which is inherent in the PLL- since phase is the integral of frequency. The HVCO gain given is for the HVCO using the KD 300 pF capacitors and the #6 powder core inductor, which is shown in the schematic.

The frequency divider is represented by a unitless constant, and is the number programmed into the feedback counter/divider on the PLL chip. It is changed slightly when different output frequencies, corresponding to voltage steps, are desired.

The open-loop small signal model is constructed by cascading the blocks given above, being sure to use Zeq for the parallel combination of HVCO input and "damping" impedances. Please note that this is just a small-signal model, so that attempts to use the blocks to compute things such as the actual high voltage output in the time domain will not work. The fact that the HVCO operates at about 2 MHz when no high voltage bias is present, for instance, is not accounted for in this model.

5. Block Diagram and Schematic

The following relates the block diagram in Figure 1 to the schematic sheets in the Attachments section.

The large dotted rectangle in the block diagram encloses several blocks contained in a single IC, U3 on sheet 1 of the schematic. This is a Motorola MC145157 frequency synthesizer chip, which provides most of the control functions for the stepper. A quartz crystal (Y1) provides a stable 10 MHz reference for the PLL system. This is typically divided down to a 1 kHz reference signal using an internal divider/counter in the MC145157. The divisor is loaded from a PC over the digital interface. In the schematic, transistors Q1 through Q3 buffer the PC printer port signals and allow for any power-up order between the PC and HV controller.

The digital interface also allows the feedback divisor to be programmed. If the loop is locked and a 1 kHz reference has been chosen, the output frequency of the HVCO (the feedback signal) will be the product of the 1 kHz reference and the feedback divisor. The feedback divisor must be chosen to allow an output frequency within the output range of the HVCO; for instance, if the HVCO free-runs near 2 MHz, divisors with values near 2000 will be needed if the reference frequency is 1 kHz. Changing the reference divisor, feedback divisor, or both will produce a change in the output frequency (which corresponds to a high voltage output change). This is how voltage steps are produced. An example BASIC PLL control program is attached to this report.

The phase detector in U3 provides "double-ended" pulse outputs (Error signal + and error signal -) which are buffered by U2, a TC4427 MOSFET driver, and used to drive LEDs in the stepper output stage. With the circuit arrangement shown, only one string of LEDs can be on at a time. Light from the LEDs causes photocurrents to be produced in the reverse-biased HV diodes (CR12-CR15) on page 3 of the schematic, in such a manner as to adjust the output voltage to a level, or "step", which causes the HVCO frequency to remain locked at a programmable multiple of the reference frequency.

Other items on page 1 of the schematic include: P1, a PC printer port connector for the digital interface; U1, a linear voltage regulator; and U4, which converts the narrow pulses from the PLL control chip into easily measurable square waves by toggling on each pulse rising edge. Q4 and LED7 provide a useful "lock detect" indication to show if the PLL is operating properly.

Page 2 of the schematic corresponds to the block labelled "HVCO With Sense Network" on the block diagram. The "sense network" is made up of C12, C13, and L1. C12 and C13 are barium titanate dielectric capacitors- just off-the-shelf, commercially available HV capacitors- which have a capacitance that varies with applied HV bias. These capacitors, along with C15, C16, and L1, form the tank of a modified Colpitts oscillator stage with Q5. Two sense capacitors and a center-tapped inductor are used so that the HV bias can be applied to an RF ground point, which keeps RF from the oscillator out of the HV system, and prevents the impedance presented by the HV stepper output from having any significant effect on the tank circuit tuning. Having a separate winding allows the tank circuit to be balanced and for the separation of the HV and control system grounds, if desired. The use of a PNP transistor for Q5 allows the "oscillator side" winding to be at DC ground as a safety precaution. The oscillator circuit is similar to variable frequency oscillator circuits used in radio equipment. The circuit shown operates near 2 MHz.

The HVCO requires a stable power supply. This is provided by U5, a linear voltage regulator. A better approach would be to use the REF02 output, both in terms of supply stability and power consumption. Q6 is an emitter follower, which allows a cable to be driven for testing the oscillator in the lab. This stage is also power hungry, and could be eliminated if short connections were made between Q5 and the frequency input on U3. The HVCO is built on a small, separate PC board to allow testing as an isolated unit.

On page 3 of the schematic are shown a high voltage converter, consisting of an oscillator/inverter (Q7 and Q8), a transformer (T1), and Cockroft-Walton multiplier stack (CR1-CR10, C27-C36) that provides "raw" high voltage DC for the system. C37 is a storage capacitor which supplies the transient (C*dv/dt) output currents required during up-steps. This corresponds to the block labelled "High Voltage Converter" in the block diagram.

The stack output is connected to diodes CR12-CR15, which, as mentioned above, act as "photodiodes" whose photocurrent is controlled by LEDs LED1-LED6. The stepper output is labelled "HV_STEP"; this is connected to the "HV_SENSE" input of the HVCO on page 2 of the schematic. R23 and C38 form a "damping" network which reduces ringing on the step output. An alternate network has been tested recently, which involved the removal of R23 and C38, and the placement of a 300 megohm resistor between the HV diodes and the HVCO input, with similar results. Note that this point in the circuit is the only place where an analog signal (the HV output) is available.

In the present system, the oscillator/inverter is biased with a current sink (U6/A), which provides a measure of short-circuit protection, but causes the converter output voltage to be unregulated. However, there is little need to tightly regulate the HV converter output; it needs only to remain a few hundred volts greater than the highest anticipated step. The current sink is adjusted (with pot RT1) to provide a "no-load" output of about 2.5 kV (as measured with a 1.0E9 ohm probe). The REF02 (U7) voltage reference is not really needed in this application, but it provides a clean reference for the current sink. U6/B provides an indication of the oscillator current.

6. HV/PLL System Critical Characteristics

It should be remembered that the output frequency of the HVCO is the actual "thing being controlled" in the PLL system. The relationship between this frequency and the HV bias on the HVCO input- the HVCO gain- is thus critical to the proper operation of the system. This is analogous to the importance of having a high quality resistive divider, whose ratio is very stable, in a conventional system. Consideration of the variation of the HVCO gain over temperature and time is very important.

Looking a bit further at the resistive divider analogy, one can see that the resistive divider case is simpler than that of the HVCO; the temperature stability and "tracking" of the two divider elements are the main considerations, if other error sources are neglected. In the HVCO, the temperature stability of the sense capacitors, the inductor, and at least three other capacitors in the circuit are all of importance. The power supply for the oscillatc should also be well-regulated.

The most important elements in the HVCO are the barium titanate "sense capacitors". The temperature coefficient of these capacitors largely determines the performance over temperature of the stepper system. It appears to be true that, in general, dielectric materials which have useful nonlinearities (relative dielectric constants which vary with applied field) also have nonzero temperature coefficients. Materials which have very temperature-stable dielectric properties show essentially no change with applied field, for practic field strengths.

Available HV capacitors are typically made of barium titanate and various additives in order to alter temperature and voltage characteristics. Usually, these characteristics are only described as being within certain tolerances by a manufacturer, so that capacitors must be characterized over temperature and applied bias by the user.

Next in importance, in terms of temperature stability, would be the core material in inductor L1. Iron powder toroids made of #6 and #7 material have been used in the HVCO circuit prototypes to date. According to the manufacturers, these materials provide a low temperature coefficient of permeability (30 to 35 ppm/degree Celsius).

The inductors have been heated to about 100 degrees Celsius for roughly 1/2 hour and allowed to cool before the windings were doped with polystyrene. This was done to "settle" the windings by giving them a thermal cycle, as suggested in an article concerning LC oscillator frequency drift [7].

The windings are trifilar, single-layer, of #24 AWG magnet wire. The cores are size T-106 (about 27 mm in diameter). These are much larger than necessary, but easy to wind and handle. The essential core properties are:

Material	Relative Permeability	Tempco ppm/degree Celsius	Effective Area [cm^2]	Effective Length [c
#6	8	35	6.50	0.69
#7	9	30	6.50	0.69

A carefully mounted air-core inductor might possibly be used, but this has not been tested. The use of a ceramic transmission line element resonator, where the inductance would be distributed on (very rigid) transmission line is also being considered; commercially available units are typically made of very temperature-stable ceramic (and therefore probably have a very low sensitivity to DC bias).

Other capacitors associated with the tank circuit, such as C15, C16, and C17 should be temperature-stable (NPO) types. If one wished to attempt to use temperature compensating capacitors to reduce frequency drift over temperature, this would be a convenient place to do so- since C15 and C16 are not subject to high voltages.

7. Prototype Power Budget

For the prototype PLL stepper circuit, the following supply current measurements were made with the output set to about 1500V:

Circuit	+15V	-15V	Power
HV Converter:	3.67 mA	-0.59 mA	63.90 mW
HVCO:	9.27 mA	N/A	139.05 mW
PLL/LED drive:	20.16 mA	N/A	302.40 mW
Totals:	33.10	-0.59 mA	505.35 mW

It should be possible to reduce the HVCO power requirements considerably, by using the REF02 to provide the stabilized +5V to operate the oscillator stage. If a short connection was made between the oscillator and PLL chip, the emitter follower stage could be omitted, saving more power. The oscillator stage alone would require about 1 mA, or 15 mW. This would reduce power use by about 124 mW. Also, the need for a negative supply could be eliminated by some minor changes in the HV converter circuit.

8. Room Temperature HVCO Test Sensitivity Test Results

The curves in Figure 5 show test results for variable-bias, room temperature tests done on three different capacitor types. A single HVCO circuit was used for these tests, and different capacitor samples soldered onto the board as needed for the tests.

The HVCO sensitivity is represented as a fraction (in parts per million per volt) of the zero-bias output frequency versus the log of the ratio of the applied bias to 1 volt. To calculate the actual output sensitivities in Hz/Volt for the three curves, use the following zero-bias frequencies:

Capacitor Sample		Zero-Bias Frequency
KD Components	300 pF, X7R, 3 kV	1.98 MHz
Maida	560 pF, X7R, 3 kV	1.62 MHz
Murata Erie	330 pF, Y5P, 3 kV	1.91 MHz

The plot was made in the above manner to compare the capacitors on a fair basis, which normalized the sensitivities to the zero bias frequency. For example, just looking roughly at the plot, the Murata Erie Y5P capacitors show a +50 ppm/V sensitivity at about 1 kV applied bias. The sensitivity in Hz/V would be:

+50 ppm/V * (1.0E-6)/ppm * 1.91 * (1.0E6) Hz = 95.5 Hz/V.

Ideally, the sensitivity for the HVCO would be a constant value for all applied bias and temperature conditions. The plot shows that the real situation is far from this; in fact, the sensitivity shows a sign change for the capacitors tested between 100V and 300V applied bias. The sensitivity sign change must be avoided during control system operation, due to stability considerations. This can be done most simply by restricting step levels either well above or below the sign change point, or by biasing the HVCO so that several hundred volts are applied to it, even when the step output is zero. The second option would complicate the system by requiring a clean source of bias, but would allow low voltage output steps to be reached.

The sensitivity sign change implies that as the HVCO bias is increased, the sense capacitance initially increases, causing the output frequency of the HVCO to drop. The capacitance increase versus applied bias becomes smaller as bias increases, however, and eventually the situation reverses, so that the sense capacitance decreases with increasing bias (in the positive portion of the sensitivity curve).

9. HVCO Temperature Tests

In order to check HVCO performance above room temperature, the HVCO was mounted in an thermally insulated box and a hot air source directed into the box for a short period (1 to 2 minutes), followed by a long period of cooling (1 hour). Temperature and frequency data were taken during the cooling period. The tests were repeated at bias levels of 0V, 500V, 1kV, 1.5kV, and 2kV. The first set of curves, Figure 6, with output frequencies in the range of 2 Mhz, was for an HVCO using the KD Components 300 pF X7R capacitors and a #6 powder cc inductor. The curves show a positive temperature coefficient of frequency.

The second set of curves, Figure 7, is for similar measurements on an HVCO containing the Maida 560 pF X7R capacitors and a #7 powder core inductor. Note the negative temperature coefficient of frequency and lower overall operating frequencies.

10. Stepper Output Tests

The final plot, Figure 8, shows stepper output voltage versus programmed frequency at room temperature. Note the near-linear characteristic of this curve, a result of negative feedback. Note also that the curve has no points below 500V. The sensitivity sign reversal of the HVCO was avoided; attempts to operate in that region resulted in an output of 0V (the "down" LEDs were driven to the maxin current). The HVCO used for this test included the KD Components 300 pF capacitors and a #6 powder core inductor.

The prototype stepper initially showed considerable ringing on the output in response to step change commands. This was improved greatly with the addition of R23 and C38 to the circuit (see sheet 3 of the schematic). An alternate approach to reduce the ringing was also tested; it involved removing R23 and C38, and putting a 300 megc resistor between the high voltage diodes and the HVCO sense capacitor The stepper prototype was slow, requiring roughly 300 ms to settle after a step change. It is felt that some things could be done to improve the prototype circuit:

(1) Use smaller sense capacitors to reduce transient output current requirements. The HVCO could also be operated at a higher frequency, and reference frequencies higher than 1 kHz used. The system bandwidt should be able to be increased with these changes.
(2) Allow larger peak currents from the LED drive stage, and improve the optical coupling between the LEDs and HV diodes. Past experience has shown that simply including transparent staking material between the LEDs and HV diodes can improve optical coupling significantly, as can careful placement of the parts. The use of surface mount parts would probably allow for tighter spacing (with due respect for high voltage conditions) and better optical coupling.
(3) Although no problems with partial discharges have been noted- at least no HVCOs have failed "mysteriously" so far- further precautions against damage from partial discharges could be implemented. Diode clamps could be applied to the HVCO output to keep output swings within a diode drop of V+ and ground, protecting other circuits. The bipolar transistor in the HVCO itself is probably rugged enough to withstand occasional partial discharge events without damage.

11. Possible Future Developments

In addition to the above recommendations for improving the circuit, a few areas of further development can be suggested. One area where improvement could be made would be in temperature calibration and compensation. With the use of a microcontroller, temperature sensor, and calibration look-up tables, the divisors sent to the PLL control IC could be adjusted to maintain HV steps close to the desired levels over a wide temperature range. A microcontroller could also be used for other supervisory functions, such as monitoring the PLL lock detect bit and reporting status or fault conditions to a host machine.

There is sometimes a desire to operate stepping supplies over wide dynamic ranges, literally from "millivolts to kilovolts". Means of extending the low voltage operating range of PLL high voltage systems need to be investigated. Providing a well-regulated bias level of several hundred volts in order avoid the "sensitivity sign change" is one possibility. A few stages of opposite-polarity rectification (with reference to the main output polarity) on a Cockroft-Walton stack, with a conventional (resistive divider) control system for regulating the bias, might be considered.

Although the use of barium titanate capacitors as voltage sensors has been emphasized in this report, this was mainly due to the fact that these were readily available. Certain additives, such as copper stannate, have been noted as making the relative dielectric constant of barium titanate even more sensitive to the applied electric field, for making "voltage-tunable capacitors" [8] (the author even mentions using such capacitors for field sensing and voltage control, but gives no details on exactly how this might have been implemented in practice). Another author mentions stannic oxide as an effective additive for making capacitors sensitive to applied bias [9]. Other materials could possibly be used as dielectrics for sense capacitors, such as titanium dioxide [10].

As capacitors are tested for use in HVCO circuits, more consideration needs to be given to whether the tests result in positive or negative coefficients of capacitance (note that this coefficient will be of the opposite sense from the frequency coefficient, if the circuit is designed so that the capacitor temperature coefficient is dominant). The importance is that if the temperature coefficient of capacitance is positive, the dielectric could show more hysteresis effects, due to being in the ferroelectric region (below the Curie point). If the temperature coefficient of capacitance is negative, the material should be operating above the Curie point, in the paraelectric region. This could be a more desirable situation from the point of step level repeatability, but needs to be tested. Examples of the effects of additives used to shift the Curie point in barium titanate are given in [11].

The effects of aging and radiation dose on the characteristics of the barium titanate capacitors would need to be considered for long-term use or in high radiation environments. Information concerning the aging of barium titanate ceramics is given in [12]. Studies concerning radiation damage in barium titanate are cited in [13].

The question of using non-ferroelectric materials for nonlinear dielectrics was raised during the course of the project. It was found that most dielectrics are nonlinear only in the case of extremely large electric fields, so large as to be impractical. A discussion of the underlying principles can be found in reference [14], and in good general references [15,16].

12. Conclusions

The primary reason for building a PLL-based high voltage control system was to demonstrate an inexpensive means of controlling a high voltage power supply with a feedback element that did not dissipate power from the high voltage converter when the output voltage was fixed. The capacitive voltage sensing used in the HVCO was one way to achieve this. Other advantages offered by the HVCO were: (1) ease of isolation of HV and control electronics grounds, and (2) the ability use it with a primarily digital control system, contained for the most part in a single IC package.

A good application for a phase-locked high voltage control system would be for driving deflection electrodes in charged particle analyzers (or other mainly capacitive loads) in situations where power dissipation needed to be minimized- as in space science payloads. Use could be considered in other applications where the output current requirements were minimal.

The operating principles and test results of a prototype high voltage system using phase-locked output control have been presented The advantages and difficulties involved in implementing such systems have been described. It is hoped that this work can provide a starting point for those wishing to apply the phase-locked control technique to their high voltage systems.

13. References

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14. Attachments

Attachment 1: Figures and Schematics

All figures and schematics described above appear in order on the following pages. Schematic sheets 1, 2 and 3 correspond to figures 2, 3, and 4, respectively.

Attachment 2: Simple PLL Control Program

The pages after the figures contain a listing of a BASIC control program used to set up the reference and feedback frequency dividers on the MC145157 PLL synthesizer chip. The program requests operator input for the crystal reference frequency, desired low frequency reference, and high frequency output. From these numbers, the divider values are computed, and then sent to the MC145157 through the PC printer port interface. The printer port signals used by this program correspond to those shown in the schematic.

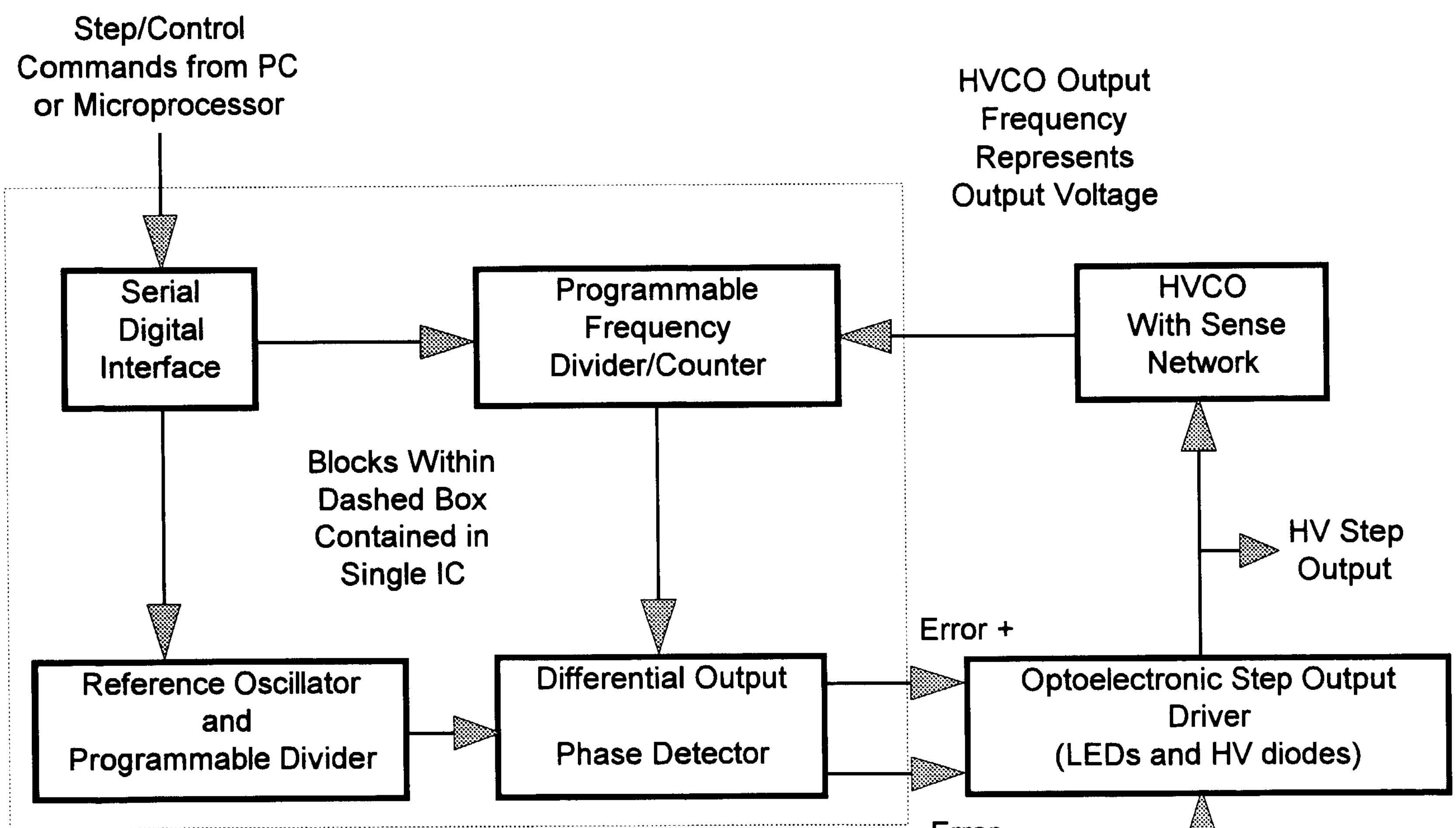
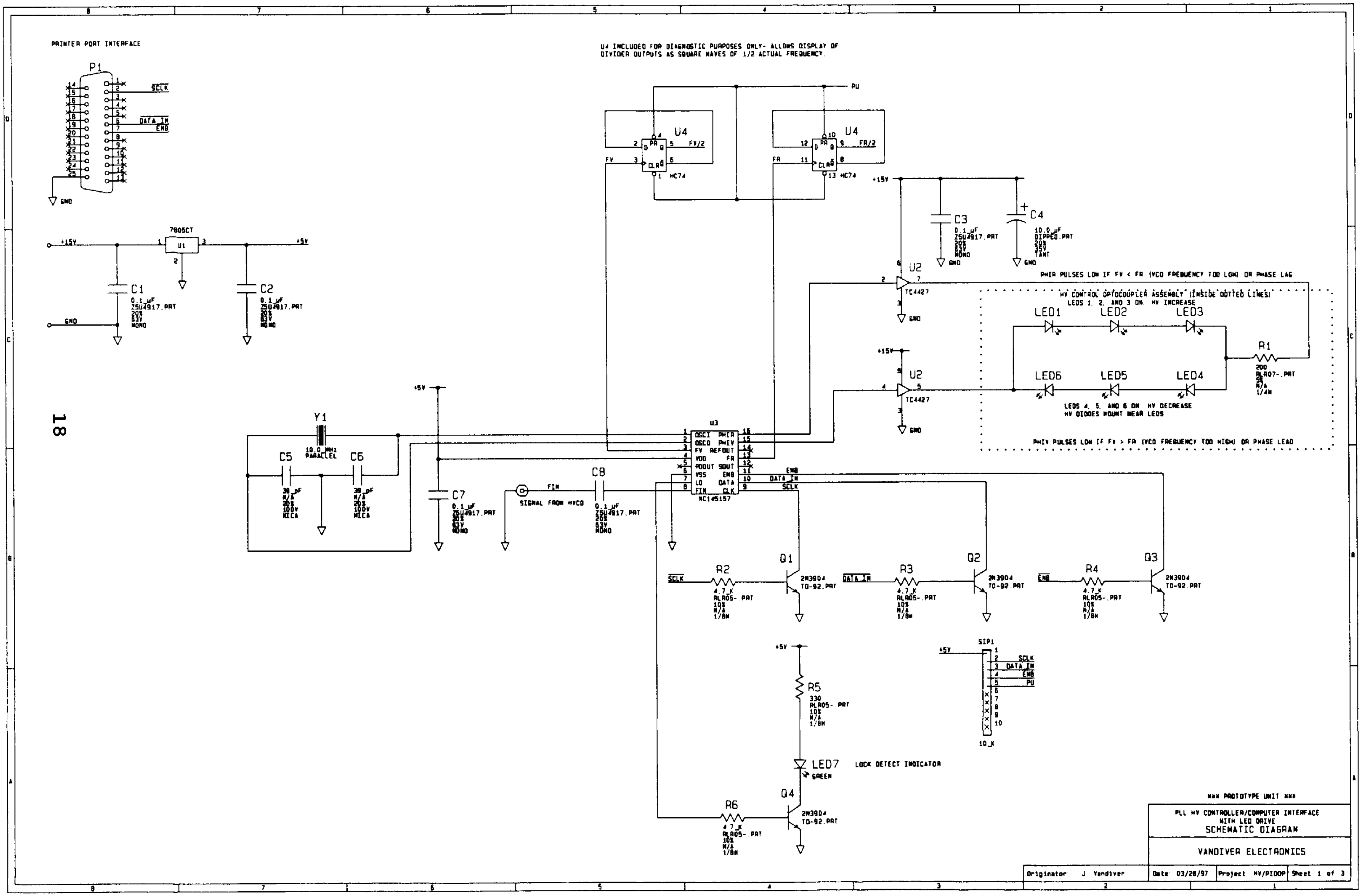
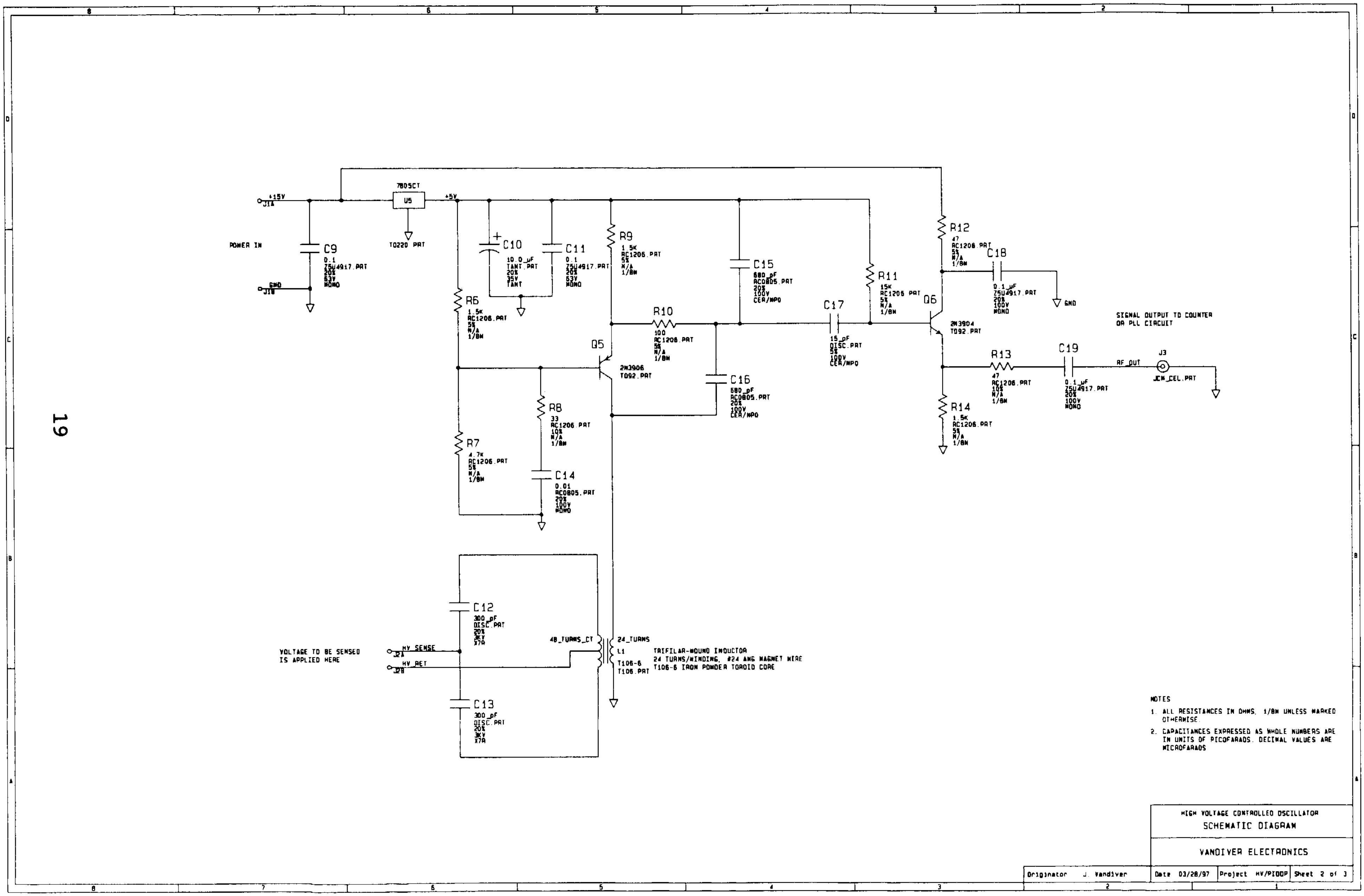
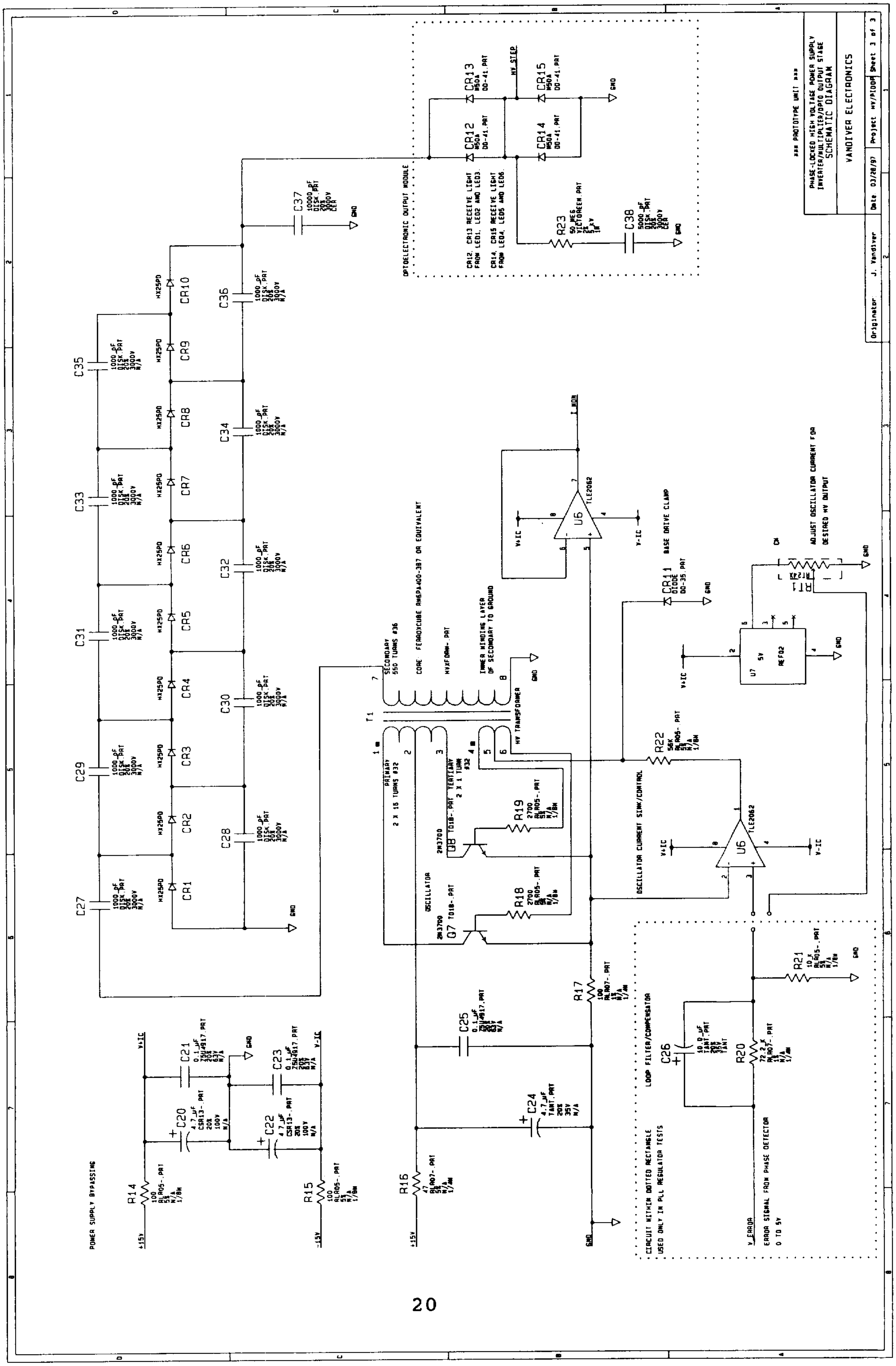


Figure 1: Phase-Locked High Voltage Control System


PRINTER PORT INTERFACE
P1
SCLK
DATA_IN
ENB
GND
7805CT
U1
+15V
+5V
C1
0.1_uF
Z5U4917.PAT
20%
63V
MONO
C2
0.1_uF
Z5U4917.PAT
20%
63V
MONO
U4 INCLUDED FOR DIAGNOSTIC PURPOSES ONLY- ALLOWS DISPLAY OF
DIVIDER OUTPUTS AS SQUARE WAVES OF 1/2 ACTUAL FREQUENCY.
PU
U4
FV/2
FR/2
HC74
FV
FR
C3
0.1_uF
Z5U4917.PAT
20%
63V
MONO
C4
10.0_uF
DIPPED.PAT
20%
35V
TANT
U2
TC4427
PHIR PULSES LOW IF FV < FR (VCO FREQUENCY TOO LOW) OR PHASE LAG
HV CONTROL OPTOCOUPLER ASSEMBLY (INSIDE DOTTED LINES)
LEDS 1, 2, AND 3 ON HV INCREASE
LED1
LED2
LED3
R1
200
RLR07-.PAT
5%
N/A
1/4W
LED6
LED5
LED4
LEDS 4, 5, AND 6 ON HV DECREASE
HV DIODES MOUNT NEAR LEDS
PHIV PULSES LOW IF FV > FR (VCO FREQUENCY TOO HIGH) OR PHASE LEAD
Y1
10.0_MHz
PARALLEL
C5
30_pF
N/A
20%
100V
MICA
C6
30_pF
N/A
20%
100V
MICA
C7
0.1_uF
Z5U4917.PAT
20%
63V
MONO
FIN
SIGNAL FROM HVCO
C8
0.1_uF
Z5U4917.PAT
20%
63V
MONO
U3
OSCI PHIR
OSCO PHIV
FV REFOUT
VDD FR
PDOUT SOUT
VSS ENB
LD DATA
FIN CLK
MC145157
R2
4.7_K
RLR05-.PAT
10%
N/A
1/8W
Q1
2N3904
TO-92.PAT
R3
Q2
R4
Q3
+5V
R5
330
RLR05-.PAT
10%
N/A
1/8W
LED7
GREEN
LOCK DETECT INDICATOR
Q4
R6
SIP1
10_X
*** PROTOTYPE UNIT ***
PLL HV CONTROLLER/COMPUTER INTERFACE
WITH LED DRIVE
SCHEMATIC DIAGRAM
VANDIVER ELECTRONICS
Originator J. Vandiver
Date 03/28/97
Project HV/PIDOP
Sheet 1 of 3


POWER IN
+15V
J1A
GND
J1B
C9
7805CT
U5
TO220.PRT
+5V
C10
C11
R6
R7
R8
R9
R10
R11
R12
R13
R14
C12
C13
C14
C15
C16
C17
C18
C19
Q5
2N3906
TO92.PRT
Q6
2N3904
TO92.PRT
GND
SIGNAL OUTPUT TO COUNTER
OR PLL CIRCUIT
J3
RF_OUT
JCN_CEL.PRT
VOLTAGE TO BE SENSED
IS APPLIED HERE
HV_SENSE
HV_RET
48_TURNS_CT
24_TURNS
L1
T106-6
T106.PRT
TRIFILAR-WOUND INDUCTOR
24 TURNS/WINDING, #24 AWG MAGNET WIRE
T106-6 IRON POWDER TOROID CORE
NOTES
1. ALL RESISTANCES IN OHMS, 1/8W UNLESS MARKED OTHERWISE.
2. CAPACITANCES EXPRESSED AS WHOLE NUMBERS ARE IN UNITS OF PICOFARADS. DECIMAL VALUES ARE MICROFARADS
HIGH VOLTAGE CONTROLLED OSCILLATOR
SCHEMATIC DIAGRAM
VANDIVER ELECTRONICS
Originator J. Vandiver
Date 03/28/97
Project HV/PIDOP
Sheet 2 of 3


*** PROTOTYPE UNIT ***
PHASE-LOCKED HIGH VOLTAGE POWER SUPPLY
INVERTER/MULTIPLIER/OPTO OUTPUT STAGE
SCHEMATIC DIAGRAM
VANDIVER ELECTRONICS
Date 03/28/97
Originator J. Vandiver
Sheet 3 of 3
POWER SUPPLY BYPASSING
OPTOELECTRONIC OUTPUT MODULE
HV TRANSFORMER
LOOP FILTER/COMPENSATOR
OSCILLATOR
BASE DRIVE CLAMP
OSCILLATOR CURRENT SINK/CONTROL

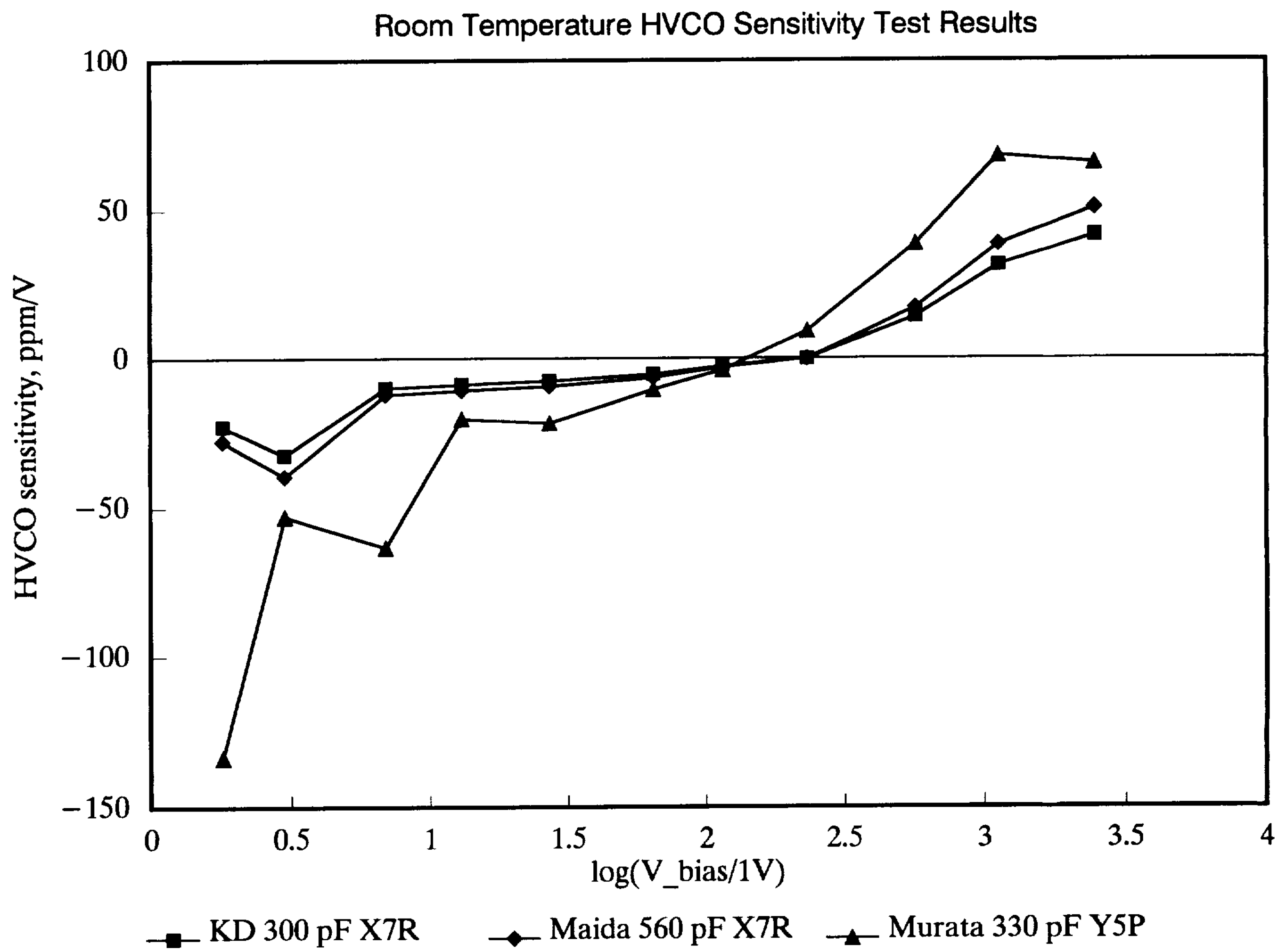
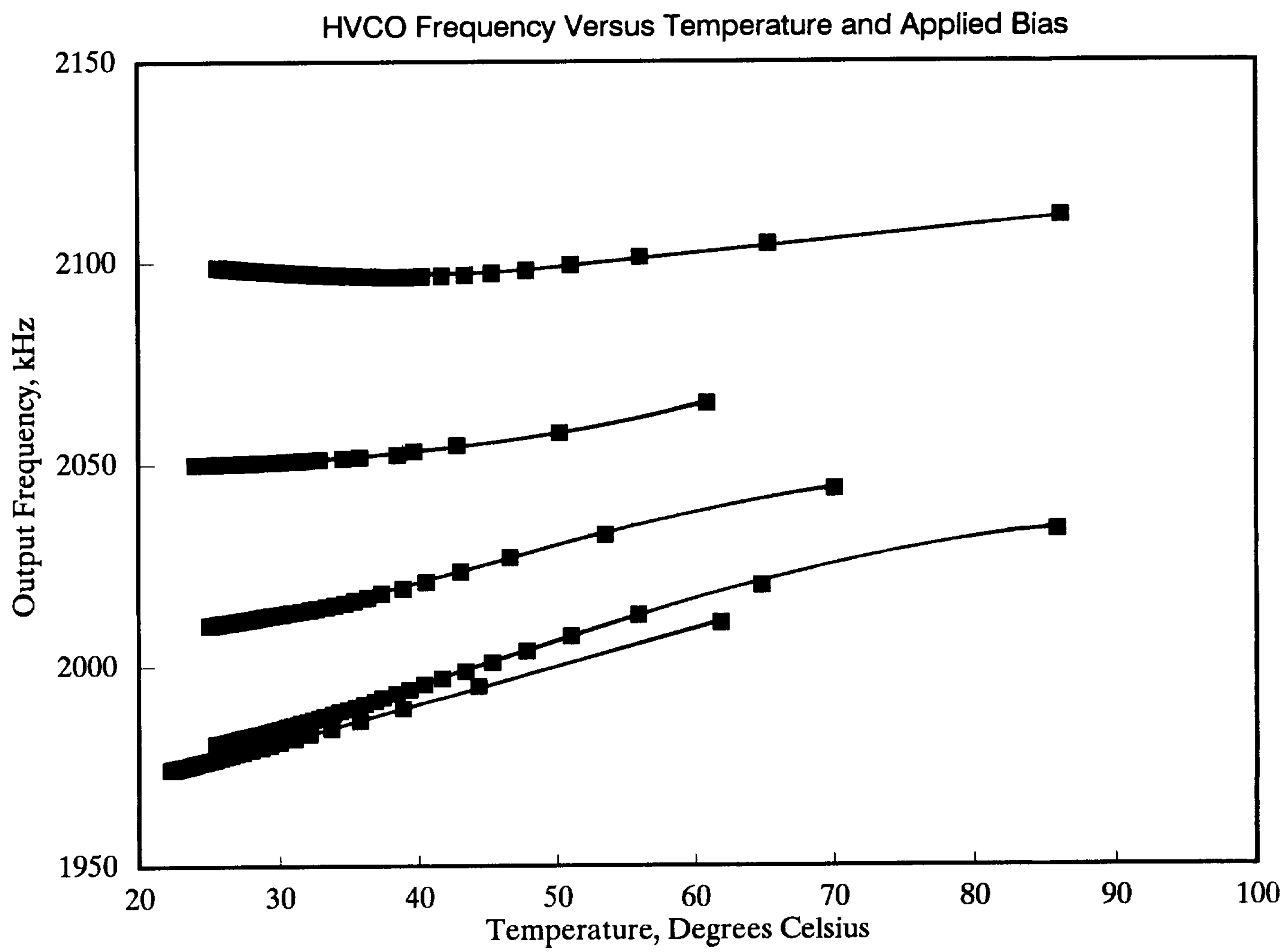

Room Temperature HVCO Sensitivity Test Results
HVCO sensitivity, ppm/V
100
50
0
−50
−100
−150
0
0.5
1
1.5
2
2.5
3
3.5
4
log(V_bias/1V)
KD 300 pF X7R
Maida 560 pF X7R
Murata 330 pF Y5P

Figure 5.



HVCO Frequency Versus Temperature and Applied Bias
2150
2100
2050
2000
1950
Output Frequency, kHz
20
30
40
50
60
70
80
90
100
Temperature, Degrees Celsius

Figure 6.

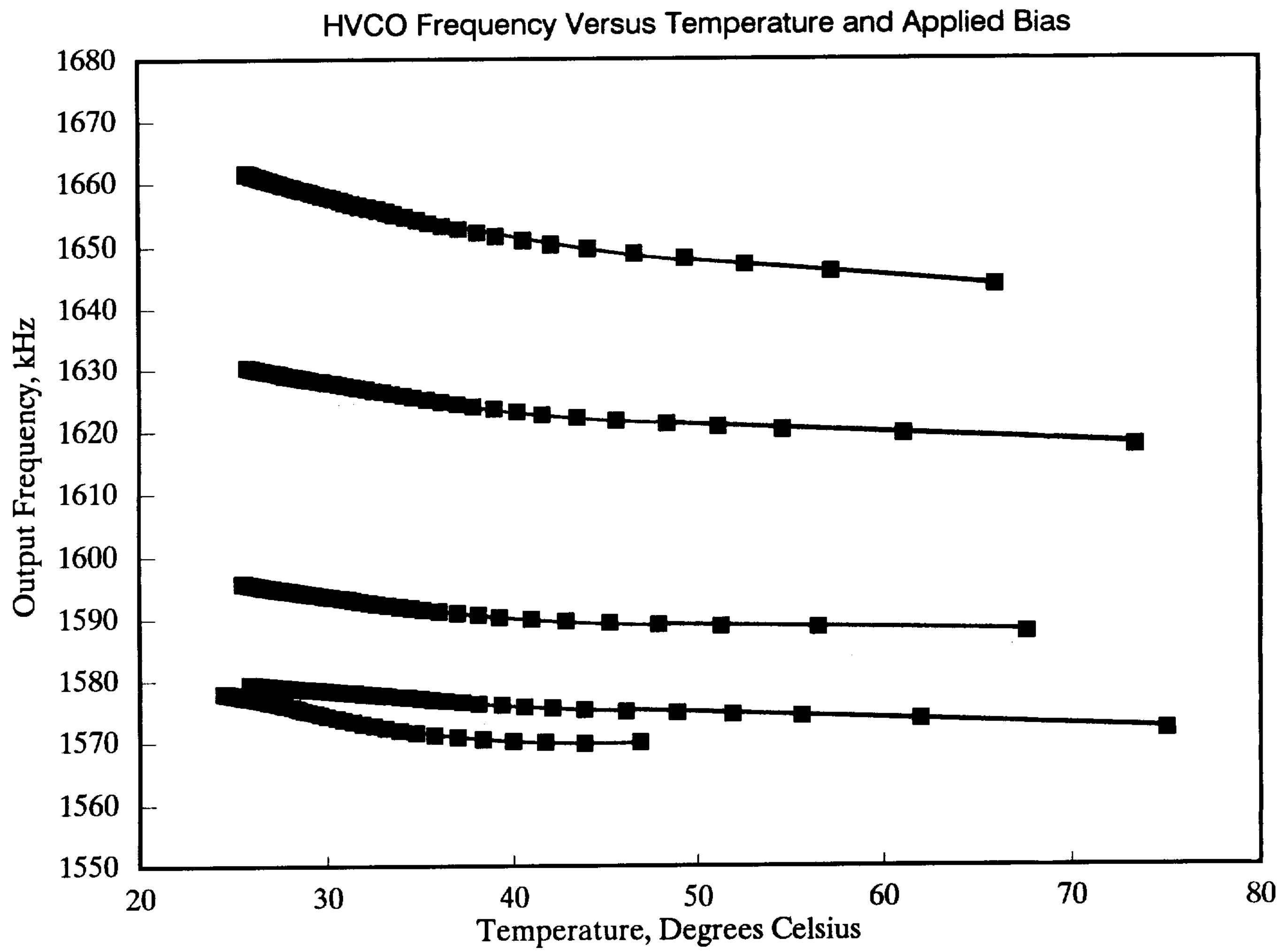
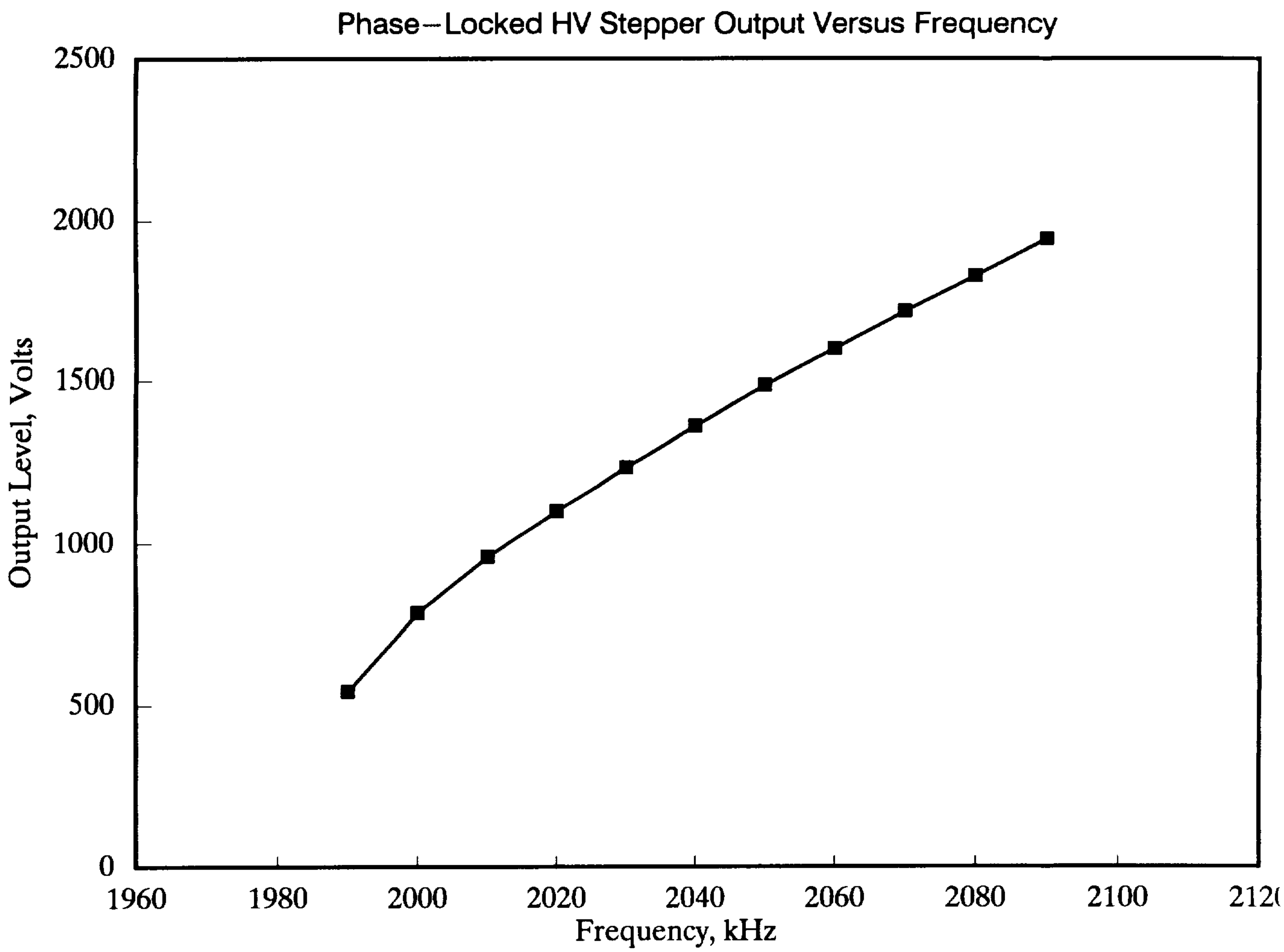

HVCO Frequency Versus Temperature and Applied Bias
1680
1670
1660
1650
1640
1630
1620
1610
1600
1590
1580
1570
1560
1550
Output Frequency, kHz
20
30
40
50
60
70
80
Temperature, Degrees Celsius

Figure 7.



Phase–Locked HV Stepper Output Versus Frequency
2500
2000
1500
1000
500
0
Output Level, Volts
1960
1980
2000
2020
2040
2060
2080
2100
2120
Frequency, kHz

Figure 8.

```
60 '*
70 ' MC145157 Frequency synthesizer control program
80 '*
90  ' Printer port bit definitions
100 DBIT = 16
110 CLOCK = 1
120 DS = 32
140 HRESET = 16
155 DPORT = 888
157 SPORT = 889
160 H$ = "0123456789ABCDEF"
165 ESC$ = CHR$(27)
172 ' Clear interface bits
175 OUT DPORT, 255
230 INPUT "Enter reference input (crystal) frequency (Hz): ", FXTAL
231 'INPUT "Enter prescaler base value (P, of P/P+1): ",P
232 INPUT "Enter reference output frequency (Hz): ",FREF
235 R = INT(FXTAL/FREF)
236 FREF = FXTAL/R
238 PRINT "Actual reference frequency: ",FREF
240 R = R*2+1
242 WORD = R\256
245 K=7
250 GOSUB 8000
252 WORD = R-256*WORD
258 K=8
260 GOSUB 8000
270 GOSUB 8150
280 INPUT "Change reference output frequency(Y/N)? ", ANS$
285 IF (ANS$="Y") OR (ANS$="y") THEN GOTO 232
300 INPUT "Enter desired output frequency (Hz), RET to quit: ", FOUT$
310 IF FOUT$="" THEN GOTO 600
315 FOUT = VAL(FOUT$)
320 D = INT(FOUT/FREF)*2
325 PRINT D/2
330 'N = D\P
340 'A = INT(D-N*P)
400 WORD = D\256
430 K=7
440 GOSUB 8000
450 WORD = D-WORD*256
480 K=8
490 GOSUB 8000
500 'WORD = A*2
530 'K=8
540 'GOSUB 8000
550 GOSUB 8150
560 GOTO 300
600 INPUT "Change reference output frequency(Y/N)? ", ANS$
610 IF (ANS$="Y") OR (ANS$="y") THEN GOTO 232
```

```
7000 '
7300 SYSTEM
7500 '
8000 ' Shift K-bit word out on printer port
8002 OUT DPORT, (CLOCK + DS)
8005 FOR I = 0 TO K-1
8010    MASK = 2 ^ (K - 1 - I)
8020    BIT = DBIT*((NOT WORD) AND MASK)\MASK
8030    OUT DPORT, (BIT + CLOCK    + DS + 0 + 0 + 0 + 0 + 0)
8040    OUT DPORT, (BIT + 0        + DS + 0 + 0 + 0 + 0 + 0)
8050 NEXT I
8060 RETURN
8065 '
8150 ' Strobe shift registers
8160 OUT DPORT, (0 + 0 + DS + 0 + 0 + 0 + 0 + 0)
8170 OUT DPORT, (0 + 0 + 0  + 0 + 0 + 0 + 0 + 0)
8175 OUT DPORT, (0 + 0 + DS + 0 + 0 + 0 + 0 + 0)
8180 RETURN
8200 END
```